

CLAIMS

What is claimed is

- 1 1. A method comprising maintaining speculative branch data for in-flight branches
2 in a speculative branch target buffer (SBTB) cache by speculatively allocating a
3 branch entry in a line of the SBTB after decoding an instruction containing a
4 branch, speculatively updating branch data associated with the branch entry after
5 branch prediction has been completed for the branch, and correcting the branch
6 data after the branch has been executed.
- 1 2. The method of claim 1, wherein the branch data includes a speculative history
2 field representing the speculative taken or not-taken history of the branch for a
3 predetermined window of executions of the branch, and wherein said
4 speculatively updating branch data comprises updating the speculative history
5 field to reflect the taken or not-taken status of its most recent execution.
- 1 3. The method of claim 1, wherein the line has a corresponding a pattern table, and
2 wherein said speculatively updating branch data comprises updating the pattern
3 table.
- 1 4. The method of claim 1, wherein the branch comprises a conditional branch.
- 1 5. The method of claim 1, wherein the branch comprises a return from a subroutine.
- 1 6. The method of claim 1, wherein the branch comprises a call to a subroutine.
- 1 7. The method of claim 1, wherein the branch comprises an unconditional branch.

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1 8. A method comprising:
2 speculatively allocating a first branch entry for a conditional branch in a
3 speculative branch target buffer (SBTB) prior to execution of the
4 conditional branch responsive to decoding the conditional branch and
5 finding no branch entry in an architectural branch target buffer (ABTB)
6 corresponding to the conditional branch;
7 speculatively allocating a second branch entry for the conditional branch in a the
8 SBTB responsive to a subsequent failed attempt to locate a branch entry in
9 the ABTB corresponding to the conditional branch;
10 allocating a third branch entry for the conditional branch in the ABTB after
11 retirement of the conditional branch; and
12 subsequently performing branch prediction for the conditional branch by
13 determining a predicted target address branch based upon branch data
14 associated with the second branch entry.

1 9. The method of claim 8, further comprising speculatively updating branch data
2 associated with the first branch entry after said performing branch prediction for
3 the conditional branch.

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- 1 10. A branch prediction circuit comprising:
2 speculative branch target buffer (SBTB) means for maintaining speculative branch
3 data associated with in-flight branches;
4 architectural branch target buffer (ABTB) means, coupled to the SBTB means, for
5 maintaining architectural branch data for branches corresponding to retired
6 instructions; and
7 target address generation means coupled to both the SBTB means and the ABTB
8 means for determining a predicted target address based upon the
9 speculative branch data and the architectural branch data.
- 1 11. The branch prediction circuit of claim 10, wherein the SBTB means comprises a
2 FIFO having entries corresponding to each of a plurality of pipeline stages of a
3 microprocessor instruction pipeline.
- 1 12. The branch prediction circuit of claim 10, wherein the SBTB means includes a
2 single read port and a single write port.
- 1 13. The branch prediction circuit of claim 10, wherein the SBTB means comprises a
2 single-ported memory.

- 1 16. A branch prediction circuit comprising:
2 a speculative branch target buffer (SBTB) cache having a plurality of branch
3 entries to maintain speculative branch data associated with in-flight
4 branches, the speculative branch data including a speculative history of
5 taken/not-taken outcomes associated with the in-flight branches; and
6 an architectural branch target buffer (ABTB) cache, coupled to the SBTB cache,
7 the ABTB cache having a plurality of branch entries to maintain
8 architectural branch data including the actual taken/not-taken outcomes
9 associated with retired conditional branches.
- 1 17. The branch prediction circuit of claim 16, wherein the SBTB cache comprises a
2 FIFO having entries corresponding to each of a plurality of pipeline stages of a
3 microprocessor instruction pipeline.
- 1 18. The branch prediction circuit of claim 16, wherein the SBTB cache is dual-ported.
- 1 19. The branch prediction circuit of claim 16, wherein the SBTB cache is single-
2 ported.
- 1 20. The branch prediction circuit of claim 16, wherein the ABTB cache is single-
2 ported.

1 21. A processor comprising:
2 a fetch unit to speculatively retrieve instruction data for processing by an
3 instruction pipeline; and
4 a branch prediction circuit, coupled to the fetch unit, to predict final target
5 addresses for branch instructions contained within the instruction data, the
6 branch prediction circuit including
7 a speculative branch target buffer (SBTB) cache having a plurality of
8 branch entries to maintain speculative branch data associated with
9 in-flight branches, the speculative branch data including a
10 speculative history of taken/not-taken outcomes associated with the
11 in-flight branches, and
12 an architectural branch target buffer (ABTB) cache, coupled to the SBTB
13 cache, the ABTB having a plurality of branch entries to maintain
14 architectural branch data including the actual taken/not-taken
15 outcomes associated with retired conditional branches.

1 22. The processor of claim 21, wherein the SBTB cache comprises a FIFO having
2 entries corresponding to each of a plurality of pipeline stages of the instruction
3 pipeline.

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